

High Density NDRO Ferroelectric Memory

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Abstract

Under a NIST ATP grant,³ Celis Semiconductor and COVA Technologies are developing very high density ferroelectric memory technology using ferroelectric transistors for the memory storage devices. The memory cell area is targeted to be comparable to that of Flash memory, but without the programming voltage scaling limitations of Flash memory. Like Flash memory, the read operation is nondestructive. The small memory cell sizes and NDRO operation provide the possibility for ferroelectric memories to replace Flash memories at the same density without resorting to die stacking techniques. Because ferroelectric storage devices are inherently tolerant to radiation exposure, ferroelectric memories using this technology in conjunction with hardened CMOS circuitry may be able to satisfy a wide range of nonvolatile semiconductor requirements for space applications.

C-V measurements on devices incorporating the ferroelectric material in the gate dielectric indicate that the programming voltage and retention time goals are reachable. Memory cell areas for various architectures range between $4F^2$ and $10F^2$, where F is the design rule feature size. The memory cell architectures simplify the process flow of the ferroelectric module and prevent perturbation of the performance of the peripheral CMOS transistors.

Design of a test chip, including memory macros, has been completed and fully processed test chips are to be completed by July 2003. To demonstrate the memory technology feasibility, the design of a small 16K prototype memory is scheduled for 2003, with fabrication and testing of the prototype memory in 2004. Commercialization of memories of 64 Mbit and larger is scheduled thereafter.

In parallel with the NIST ATP project, implementation of this technology on SOI wafers is being evaluated under an MDA SBIR grant.⁴

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